SC11805TP

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*			Application Number	
			Filing Date	
			First Named Inventor	Leo Mathew
			Group Art Unit	
			Examiner Name	
Sheet	1	of	1	Attorney Docket Number	SC11805TP

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	AA	Jerry G. Fossum et al., "Extraordinarily high drive currents in asymmetrical double-gate", Superlattices and Microstructures, Vol. 28, No. 5/6, 2000, 2000 Academic Press, pgs. 525-530.	
	AB	Tetsu Tanaka et al., "Ultrafast Operation of Vth-Adjusted p+-n+ Double-Gate SOI MOSFET's, IEEE Electron Device Letters, Vol. 15, No. 10, October 1994, pgs. 386-388.	
	AC	Keunwoo Kim et al., "Double-Gate CMOS: Symmetrical – Versus Asymmetrical-Gate Devices", IEEE Transactions On Electron Devices, Vol. 48, No. 2, February 2001, pgs. 294-299.	
	AD	Digh Hisamoto et al., "FinFET – A Self-Aligned Double-Gate MOSFET Scalable to 20 nm", IEEE Transactions On Electron Devices, Vol. 47, No. 12, December 2000, pgs. 2320-2325.	
	AE	Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies", 2001 IEEE, website:ykchoi@eecs.Berkeley.edu, 4 pages.	
	AF	Jakub Kedzierski et al., "High-performance symmetric-gate and CMOS-compatible Vt asymmetric-gate FinFET devices", 2001 IEEE, 4 pages.	

Examiner Signature		Date Considered	9/5/2003

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation, if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] Unique citation designation number. [2] Applicant is to place a check mark here if English Language Translation is attached.